REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicants replace the Abstract as required by the Examiner, and amend claims 35 and 38 to correct typographical and other minor errors which occurred while transcribing the claims for the Preliminary Amendment filed together with this continuation application.

Accordingly, claims 21-42 are pending in the application.

Reexamination and reconsideration are respectfully requested in view of the following remarks.

35 U.S.C. § 102 and 103

The Office Action rejects: claims 21-42 under 35 U.S.C. § 102 over Baji U.S. Patent 5,513,374; and claims 35-40 under 35 U.S.C. § 103 over Baji in view of Upender et al. U.S. Patent 5,854,454 ("Upender").

Applicants respectfully traverse these rejections for at least the following reasons.

Claim 21

Among other things, the microcontroller of claim 21 supports a plurality of message objects and includes: (1) a processor core that runs applications; (2) a module that processes incoming messages; and (3) data memory including a first memory segment that provides a plurality of message buffers associated with respective ones of the message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object.

Applicants respectfully submit that Baji does not disclose this combination of features.

In particular, the microcontroller of claim 21 includes a data memory having a first memory segment that provides a plurality of message buffers associated with respective message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped

registers for each message object containing respective command/control fields for configuration and setup of that message object.

Applicants respectfully submit that Baji does not disclose any microcontroller including a data memory with these recited features.

The Office Action states that both data memory 1900 and instruction memory 1400 correspond to the recited first memory segment that includes a plurality of message buffers associated with respective message objects, and also states that instruction memory 1400 corresponds to the second memory segment that includes a plurality of memory-mapped registers for each of the message objects.

Applicants respectfully disagree.

At the outset, instruction memory 1400 of Baji is just that – an ***instruction*** memory for storing instructions. Baji does not disclose that includes either a plurality of message buffers associated with any the message objects, or a plurality of memory-mapped registers for message objects . . . as surely it doesn't. Indeed, the Office Action does not cite anything in Baji that even allegedly discloses that instruction memory 1400 (or data memory 1900, for that matter), includes either a plurality of message buffers associated with any the message objects, or a plurality of memory-mapped registers for message objects.

Therefore, Baji cannot disclose the microcontroller of claim 21.

Also, and more specifically, in the microcontroller of claim 21, the memory-mapped registers of the second memory segment for each message object contain respective command/control fields for configuration and setup of that message object.

Applicants respectfully submit that Baji does not disclose any microcontroller including the recited memory-mapped registers with these features.

The Office Action cites col. 5, lines 54-64 of Baji as supposedly disclosing the recited memory-mapped registers with these features. Reproduced below is the text of Baji at col. 5, lines 54-64:

> In this DSP **1100**, virtually all resources, including registers, internal memories, external memories, internal interfaces to peripheral devices, and the like are "memory mapped", meaning that each such resource has a predefined, unique, address. Both the DMAC **3000** and the DSP Core **3500** can independently access almost all memory mapped locations in the external memory **2500**, instruction memory **1400**, peripheral devices **2300** or data memory **1900** as well as most of the internal registers. By memory mapping all DSP resources, the DSP **1100** also makes all memory mapped resources accessible to the host processor **1200**.

Nowhere in this text does it disclose that instruction memory 1400 includes a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object. Indeed, the cited text does even not mention any command/control fields or message objects!

Therefore, Baji cannot disclose the microcontroller of claim 21.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 21 is patentable over the prior art.

Claims 22-27

Claims 22-27 depend from claim 21 and are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 21, and for the following additional reasons.

Claim 22

Among other things, in the microcontroller of claim 22 the incoming messages include multi-frame, fragmented messages, and the module automatically assembles the multi-frame, fragmented messages.

Applicants respectfully submit that Baji does not disclose such features.

The Office Action states that figure 4 shows multi-frame fragmented instructions handled by the DMAC.

Applicants respectfully disagree.

Indeed, Baji does not include a "figure 4" but instead includes FIGS. 4A-4E (with FIG. 4A including six separate sheets) which Baji states disclose block diagrams . . . not any multi-frame, fragmented messages, automatically assembled by DMAC 3000.

Accordingly for at least this additional reason, claim 22 is deemed patentable over Baji.

Claim 24

Among other things, in the microcontroller of claim 24, the processor core, the module, and the memory interface unit are contained on a single integrated circuit chip.

Applicants respectfully submit that Baji does not disclose such features.

The Office Action states that such a feature is shown in FIG. 1

Applicants respectfully disagree.

Not only does FIG. 1 of Baji fail to show that elements 1200 and 3000 are contained on a single integrated circuit chip, but FIGs. 4B and 4D, and the text at col. 21, line 25 – col. 22, line 24 (specifically col. 21, lines 25-26) all indicate that the host microprocessor 1200 is ***not*** contained on a same chip as DMAC 3000.

Accordingly for at least these additional reasons, claim 24 is deemed patentable over Baji.

Claim 27

Among other things, in the microcontroller of claim 27, the memory interface unit arbitrates access according to an alternate winner policy, wherein a previous loser is designated a current winner.

Applicants respectfully submit that Baji does not disclose such a feature. In particular, Applicants respectfully submit that Baji does not disclose such a feature at col. 7, lines 1-34.

Accordingly for at least this additional reason, claim 27 is deemed patentable over Baji.

Claim 28

Among other things, in similarity to claim 21, microcontroller of claim 28

includes: (1) a processor core that runs applications; (2) a module that processes incoming messages; and (3) data memory including a first memory space that is located on the integrated circuit chip and a second memory space that is located off the integrated circuit chip, the first memory space including a first memory segment that provides at least a portion of a message buffer memory space that includes a plurality of message buffers associated with respective ones of the message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object.

As explained above with respect to claim 1, Baji does not disclose data memory including a first memory segment that provides at least a portion of a message buffer memory space that includes a plurality of message buffers associated with respective message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object.

Therefore, Baji cannot disclose the microcontroller of claim 28.

Also, in the microcontroller of claim 28, a processor core that runs applications, and the module that processes incoming messages, are contained on a single integrated circuit chip.

Applicants respectfully submit that Baji does not disclose such a feature.

The Office Action states that the processor core of Baji includes host processor 1200, and the module corresponds to DMAC 3000.

However, the Office Action does not cite any text in Baji that discloses that elements 1200 and 3000 are contained on a single integrated circuit chip. And clearly no such feature is disclosed in FIG. 1 Indeed, FIGs. 4B and 4D, and the text at col. 21, line 25 – col. 22, line 24 (specifically col. 21, lines 25-26) all indicate that the host microprocessor is ***not*** contained on a same chip as DMAC 3000.

Accordingly, for at least these reasons, Applicants respectfully submit that

claim 28 is patentable over the prior art.

Claims 29-34

Claims 29-34 depend from claim 28 and are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 28. Furthermore, claims 29 and 34 are also deemed patentable for the reasons set forth above with respect to similar claims 22 and 27, respectively.

Claim 35

Among other things, the method of claim 35 includes permitting a processor core and a module to concurrently access a different respective one of a first memory segment that provides at least a portion of a message buffer memory space that includes a plurality of message buffers associated with respective message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object.

As explained above with respect to claims 21 and 28, Baji does not provide access to any such first and second memory segments.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 35 is patentable over Baji.

Claims 36 and 37

Claims 36 and 37 depend from claim 35 and are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 35. Furthermore, claim 36 is also deemed patentable for the reasons set forth above with respect to similar claim 27.

Claim 38

Among other things, the method of claim 38 includes permitting a processor core and a module to concurrently access a different respective one of a first memory segment that provides at least a portion of a message buffer memory space that includes a plurality of message buffers associated with respective message objects, and a second memory segment that provides a plurality of memory-mapped

registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object.

As explained above with respect to claims 21, 28 and 35, Baji does not provide access to any such first and second memory segments.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 38 is patentable over Baji.

Claims 39 and 40

Claims 39 and 40 depend from claim 38 and are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 38. Furthermore, claim 39 is also deemed patentable for the reasons set forth above with respect to similar claim 27.

Claim 41

Among other things, the bus station of claim 41 includes a microcontroller that supports a plurality of message objects and includes: (1) a processor core that runs applications; (2) a module that processes incoming messages; and (3) data memory including a first memory segment that provides a plurality of message buffers associated with respective ones of the message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object.

As explained above with respect to claim 21, Baji does not include any microcontroller with this combination of features.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 41 is patentable over Baji.

Claim 42

Among other things, the bus system of claim 42 includes a microcontroller that supports a plurality of message objects and includes: (1) a processor core that runs applications; (2) a module that processes incoming messages; and (3) data memory

including a first memory segment that provides a plurality of message buffers associated with respective ones of the message objects, and a second memory segment that provides a plurality of memory-mapped registers for each of the message objects, the memory-mapped registers for each message object containing respective command/control fields for configuration and setup of that message object.

As explained above with respect to claim 21, Baji does not include any microcontroller with this combination of features.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 42 is patentable over Baji.

Claims 35-40 Are Also Patentable over Baji and Upender

Apparently, the alternate rejections of claims 35-40 under 35 U.S.C. § 103 over Baji in view of Upender were made in view of some typographical errors in claims 35 and 38 as originally filed.

By this Amendment, Applicants amend claims 25 and 38 to delete the inadvertent references to CAN and CAL. Therefore, it is believed that the rejections of claims 35-40 under 35 U.S.C. § 103 over Baji in view of Upender are now moot. Accordingly, Applicants see no need to discuss whether Baji and Upender are even properly combinable as proposed.

In any event, Applicants respectfully submit that Upender does not remedy the shortcomings of Baji with respect to claims 35-40, as set forth above.

Accordingly, claims 35-40 are deemed patentable over any possible combination of Baji and Upender.

OBVIOUSNESS-TYPE DOUBLE-PATENTING REJECTIONS

The Office Action rejects claims 21-42 on the ground of obviousness-type double patenting over U.S. patents 6,715,001, 6,732,255, 6,498,287, and 6,647,440.

The Office Action fails to state any reasons why it is believed that claims 21-42 are not patentably distinct from the claims of any of the U.S. patents 6,715,001,

6,498,287, and 6,647,440. Accordingly, at this time Applicants respectfully traverse those rejections until and unless an explanation is provided as to why it is believed that claims 21-42 of the present application are not patentably distinct from the claims of these patents. Meanwhile, with respect to U.S. patent 6,732,255, Applicants are prepared to submit a terminal disclaimer if and when the claims of the present application are declared to be otherwise patentable, and therefore not subject to need for any amendment.

CONCLUSION

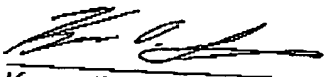
In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 21-42 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment (except for the issue fee) to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

Date: 19 December 2006

By: 
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